REMARKS

Claims 1-7, 10-15 and 25-28 remain pending. Claims 8-9 and 16-17 have been canceled without prejudice or disclaimer. New claims 27 and 28 have been added.

35 U.S.C. §102

Claims 1-17, 25 and 26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Ota (U.S. Patent Publication No. 2002/0047170). This rejection is traversed as follows.

The present invention is directed to a method of manufacturing a semiconductor integrated circuit device in which a high dielectric constant insulating film is removed before implantation of an impurity to form which constitutes a semiconductor region, extension region and Halo layer. Therefore, the impurity implanting characteristic of the semiconductor region is improved. When the high dielectric constant insulating film is not removed, the implantation energy has to be increased, which broadens the profile of the impurity. This makes it more difficult to implant the impurity with as much control as would be possible if the high dielectric constant insulating film had been removed.

The claims have been amended to clarify this feature of the present invention. On the other hand, Ota discloses that while sidewalls 16 on the sides of a gate-shaped polysilicon layer 4 are formed, a hard mask pattern 5a is removed as well as $HfSiO_2$ film 21, HfO_2 film 22 and $HfSiO_2$ film 23. These insulating films 21, 22 and

23 are removed except for portions under polysilicon layer 4 and sidewalls 16 (see Fig. 16 and [0090]). Therefore, as shown in Fig. 14, impurity ions 19 are implanted into the substrate through insulating films 21, 22 and 23, thereby reducing the impurity implanting characteristic. In addition, the capacitance between the source/drain region 8, 9 and the gate electrode 4 is increased thereby reducing an operation characteristic of the device. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

Request for Interview

Applicants request that the Examiner conduct an interview with the undersigned in order to expedite prosecution of this application. In this regard, the Examiner is hereby invited to contact the undersigned by telephone in order to arrange an appropriate time for the interview.

Conclusion

In view of the foregoing, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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